LISTING OF THE CLAIMS

A detailed listing of claims is presented below. Please amend currently amended claims as indicated below including substituting clean versions for pending claims with the same number. In addition, clean text versions of pending claims not being currently amended that are under examination are also presented. It is understood that any claim presented in a clean version below has not been changed relative to the immediate prior version.

1. (Currently Amended) A display unit comprising:

a display panel comprising a pixel matrix comprising: an (m x n) pixel frame buffer region; and an x pixel border region for only displaying a display attribute, wherein said border region surrounds said frame buffer region;

a frame buffer memory for containing image data for generating an image within said frame buffer region;

a border attribute register for containing said display attribute for said border region, wherein said display attribute is automatically selected to provide viewing contrast with image data located near said border region; and

a display controller coupled to said frame buffer memory, coupled to receive said display attribute from said border attribute register, and coupled to control said display panel, said display controller for generating a first set of signals for rendering said image within said frame

buffer region and for generating a second set of signals for displaying said display attribute within said border region.

2. (Original) A display unit as described in Claim 1 wherein said second set of signals are generated within invalid timing windows with respect to said frame buffer region.

3. (Original) A display unit as described in Claim 1 wherein a first portion of said second set of signals are generated in an invalid horizontal timing window that commences x clock cycles before valid data for said frame buffer region commences and wherein a second portion of said second set of signals are generated in an invalid horizontal timing window that ends x clock cycles after valid data for said frame buffer region completes.

4. (Original) A display unit as described in Claim 3 wherein a third portion of said second set of signals are generated in an invalid vertical timing window that commences x horizontal pulses before a first valid horizontal line commences of a frame and wherein a forth portion of said second set of signals are generated in an invalid vertical timing window that ends x horizontal pulses after the end of the last valid horizontal line of said frame.

5. (Original) A display unit as described in Claim 1, wherein said display attribute of said border region comprises a color attribute and an intensity attribute.

6. (Original) A display unit as described in Claim 1 wherein said display panel is a thin film transistor liquid crystal display panel.

7. (Original) A display unit as described in Claim 1 wherein x=2.

8. (Original) A display unit as described in Claim 1 wherein said frame buffer region comprises 160 rows and 160 columns of pixels.

9. (Original) A display unit as described in Claim 1 further comprising a background display attribute register and wherein, by default, said border attribute register is equal to said background attribute register.

10. (Currently Amended) A display unit comprising:

a display panel comprising a pixel matrix comprising: an (m x n) pixel frame buffer region; and an x pixel border region for only displaying a display attribute, wherein said border region surrounds said frame buffer region and contains top, bottom, right and left border regions;

a frame buffer memory for containing character data for generating character images within said frame buffer region;

a border attribute register for containing said display attribute for said border region, wherein said display attribute is automatically selected to provide viewing contrast with character images located near said border region; and

a display controller coupled to said frame buffer memory, coupled to receive said display attribute of said border attribute register, and coupled to control said display panel, said display controller for generating a first set of signals for rendering said character images within said frame buffer region wherein said first set of signals comprises vertical and horizontal invalid timing windows and wherein said display controller is also for generating a second set of signals for displaying said display attribute within said border region.

11. (Original) A display unit as described in Claim 10 wherein said second set of signals are generated within said vertical and horizontal invalid timing windows.

12. (Original) A display unit as described in Claim 10 wherein said top and bottom border regions are rendered during said vertical invalid timing windows and wherein said right and left border regions are rendered during said horizontal invalid timing windows.

13. (Original) A display unit as described in Claim 10 wherein said display attribute comprises a color attribute and an intensity attribute.

14. (Original) A display unit as described in Claim 10 wherein said display panel is a thin film transistor liquid crystal display panel.

15. (Original) A display unit as described in Claim 10 wherein x=2.

16. (Original) A display unit as described in Claim 10 wherein said frame buffer region comprises 160 rows and 160 columns of pixels.

17. (Original) A display unit as described in Claim 10 further comprising a background display attribute register and wherein, by default, said border attribute register is equal to said background attribute register.

18. (Currently Amended) A portable electronic device comprising:

a processor coupled to a bus;

a memory unit coupled to said bus;

a user input device coupled to said bus; and

a display unit coupled to said bus and comprising:

a display panel comprising a pixel matrix comprising: an (m x n) pixel frame buffer region; and an x pixel border region for only displaying a display attribute, wherein said border region surrounds said frame buffer region;

a frame buffer memory for containing image data for generating an image within said frame buffer region;

a border attribute register for containing said display attribute for said border region, wherein said display attribute is automatically selected to provide viewing contrast with image data located near said border region; and

a display controller coupled to said frame buffer memory, coupled to receive said display attribute from said border attribute register, and coupled to control said display panel, said display controller for generating a first set of signals for rendering said image within said frame buffer region and for generating a second set of signals for displaying said display attribute within said border region.

19. (Original) A portable electronic device as described in Claim 18 wherein said second set of signals are generated within video timing windows that contain invalid data with respect to said frame buffer region.

20. (Original) A portable electronic device as described in Claim 18 wherein a first portion of said second set of signals are generated x clock cycles before valid data for said frame buffer region commences and wherein a second portion of said second set of signals are generated x clock cycles after valid data for said frame buffer region completes.

21. (Original) A portable electronic device as described in Claim 18 wherein said display attribute comprises a color attribute and an intensity attribute.

22. (Original) A portable electronic device as described in Claim 18 wherein said display panel is a thin film transistor liquid crystal display panel.

23. (Original) A portable electronic device as described in Claim 18 further comprising a background display attribute register and wherein, by default, said border attribute register is equal to said background attribute register.